

FIG. 1

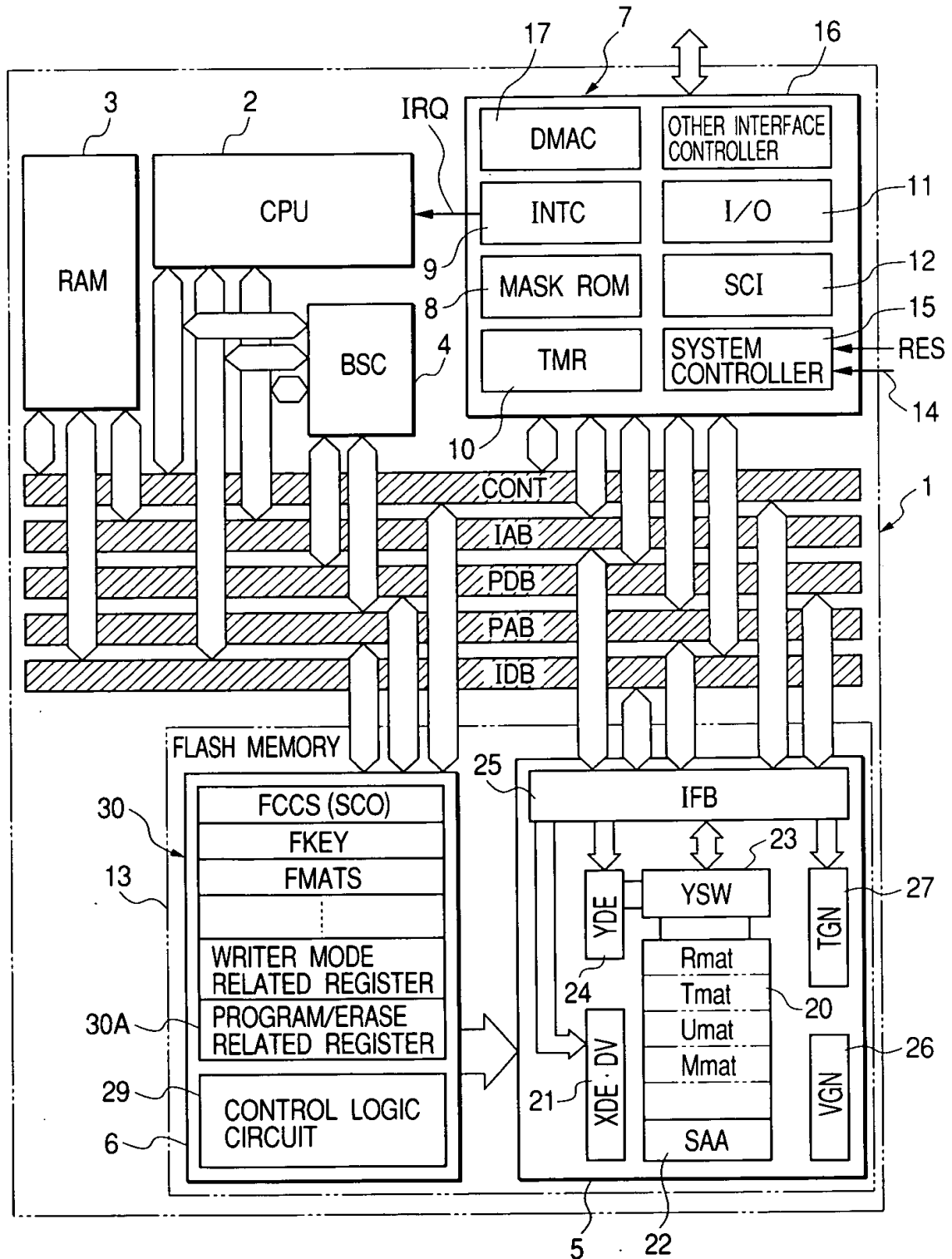


FIG. 2

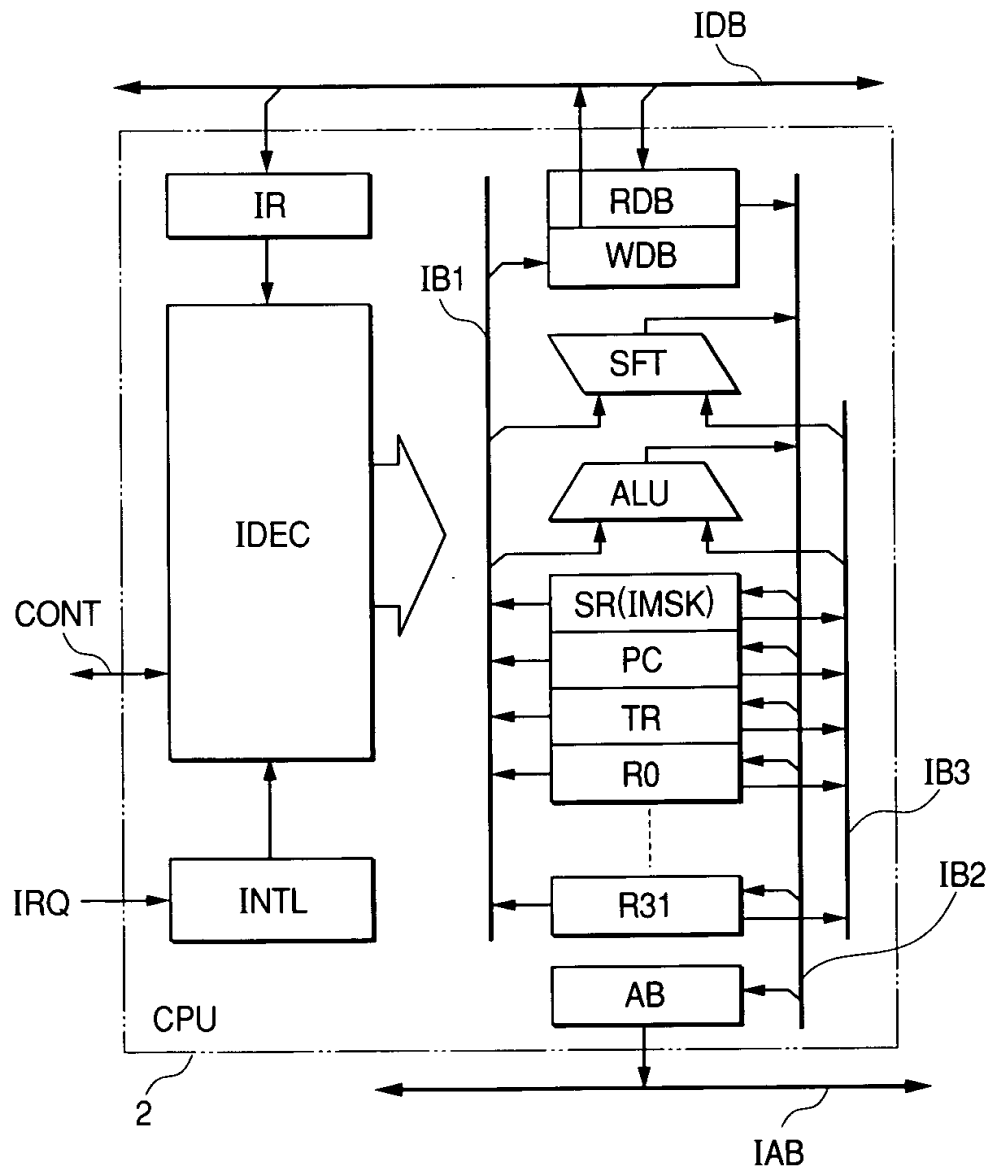
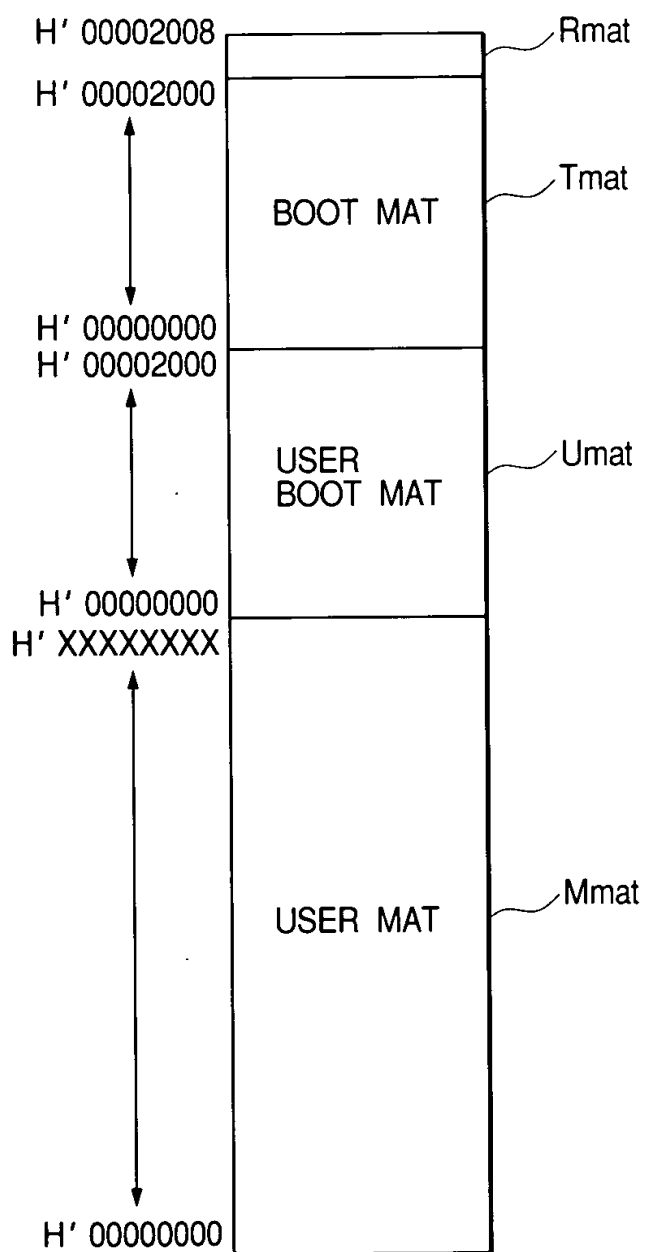


FIG. 3

20000000 00000000

FIG. 4(A)

OPERATION MODE MAT	BOOT MODE			WRITER MODE		
	ACCESS	PROGRAM	ERASE	ACCESS	PROGRAM	ERASE
USER MAT (Mmat)	○	○	○	○	○	○
USER BOOT MAT (Umat)	○	○	○	○	○	○
BOOT MAT (Tmat)	△	x	x	△	x	x
REPAIR & TRIMMING (Rmat)	x	x	x	x	x	x

FIG. 4(B)

OPERATION MODE MAT	USER BOOT MODE			USER MODE		
	ACCESS	PROGRAM	ERASE	ACCESS	PROGRAM	ERASE
USER MAT (Mmat)	○	○	○	○	○	○
USER BOOT MAT (Umat)	○	x	x	○	x	x
BOOT MAT (Tmat)	△	x	x	△	x	x
REPAIR & TRIMMING (Rmat)	x	x	x	x	x	x

FIG. 5

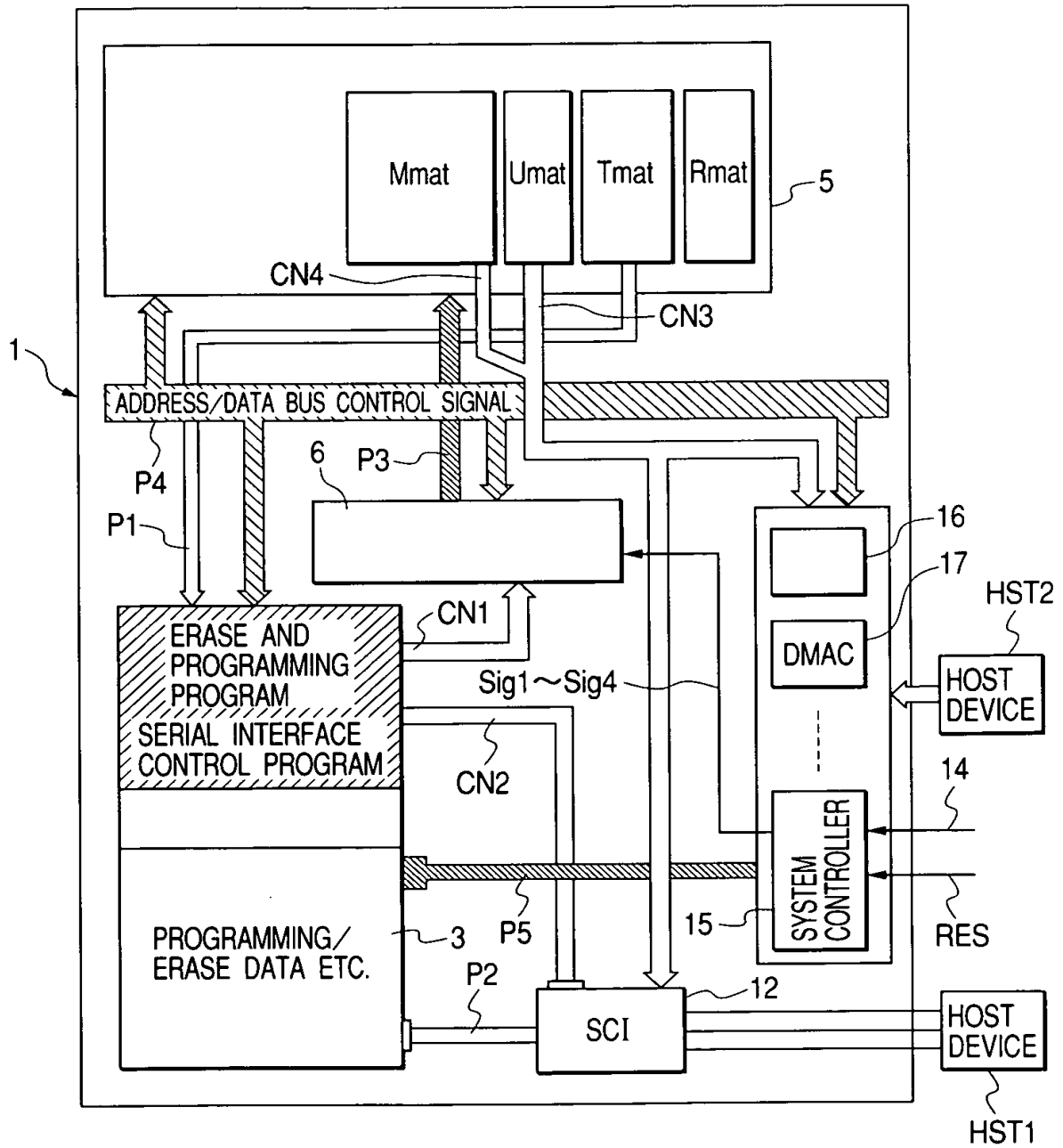


FIG. 6

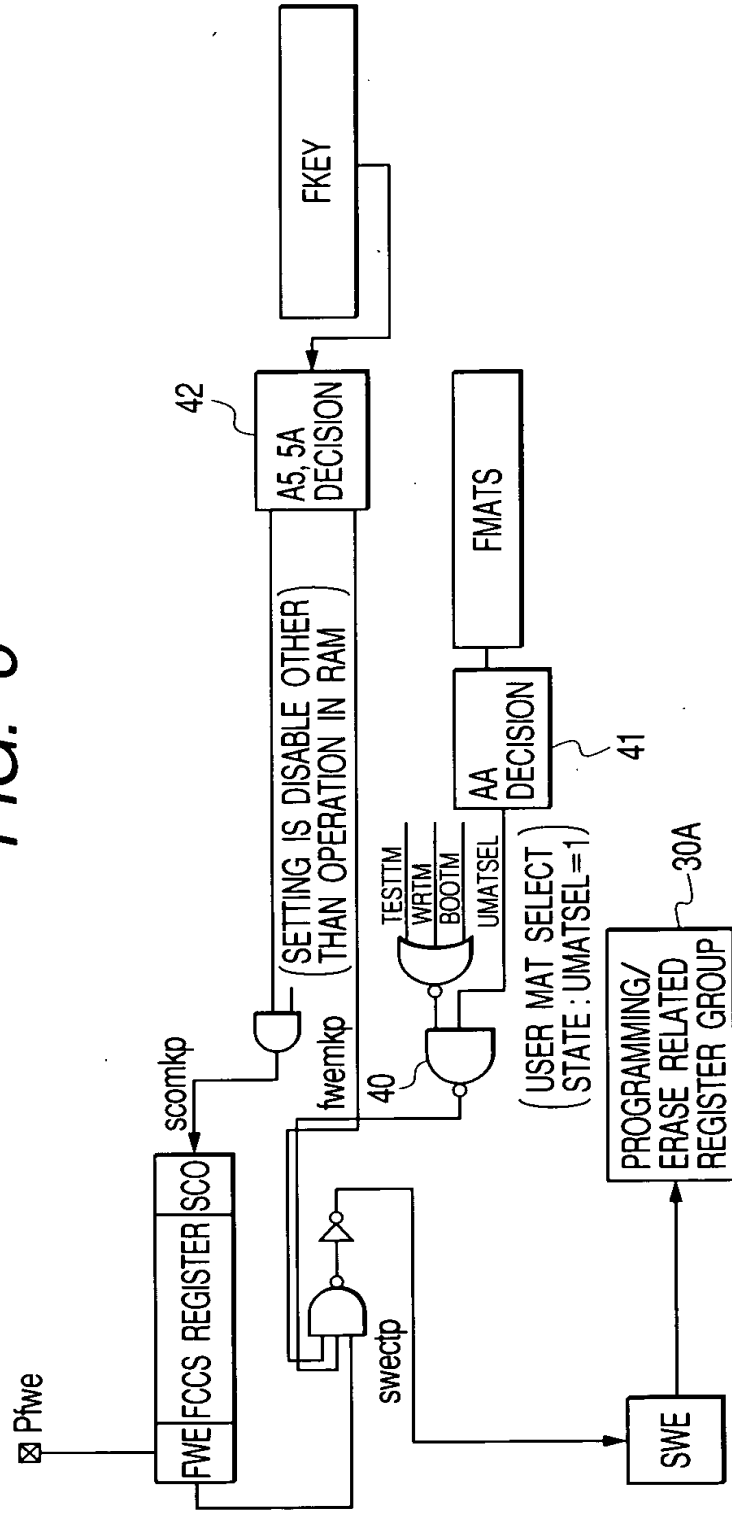
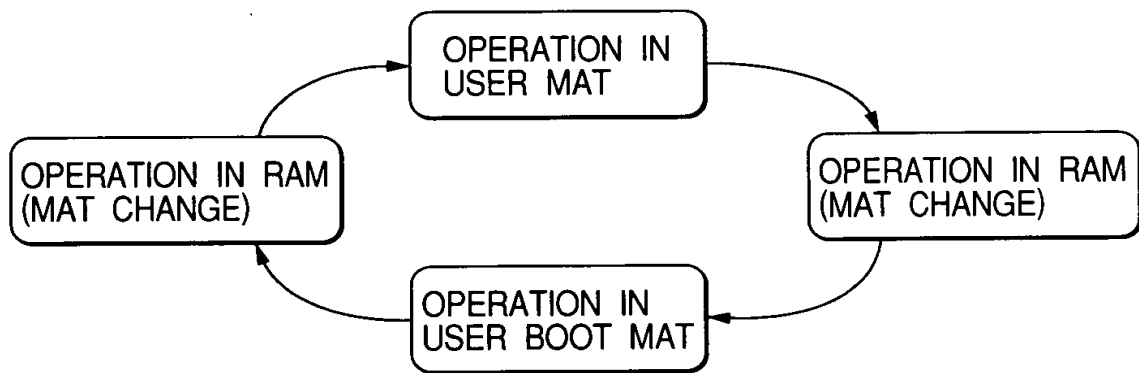


FIG. 7



2025 RELEASE UNDER E.O. 14176

FIG. 8

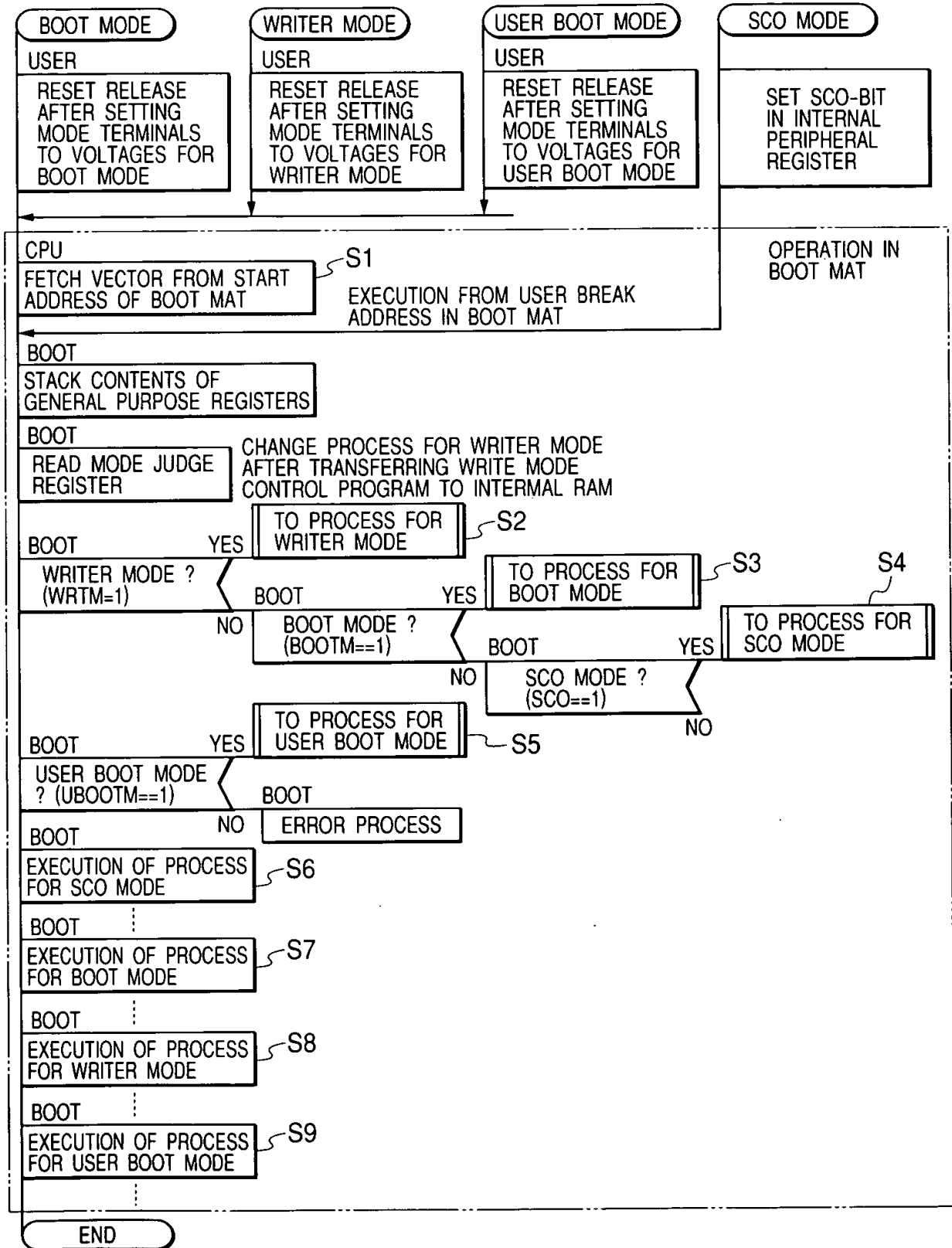


FIG. 9

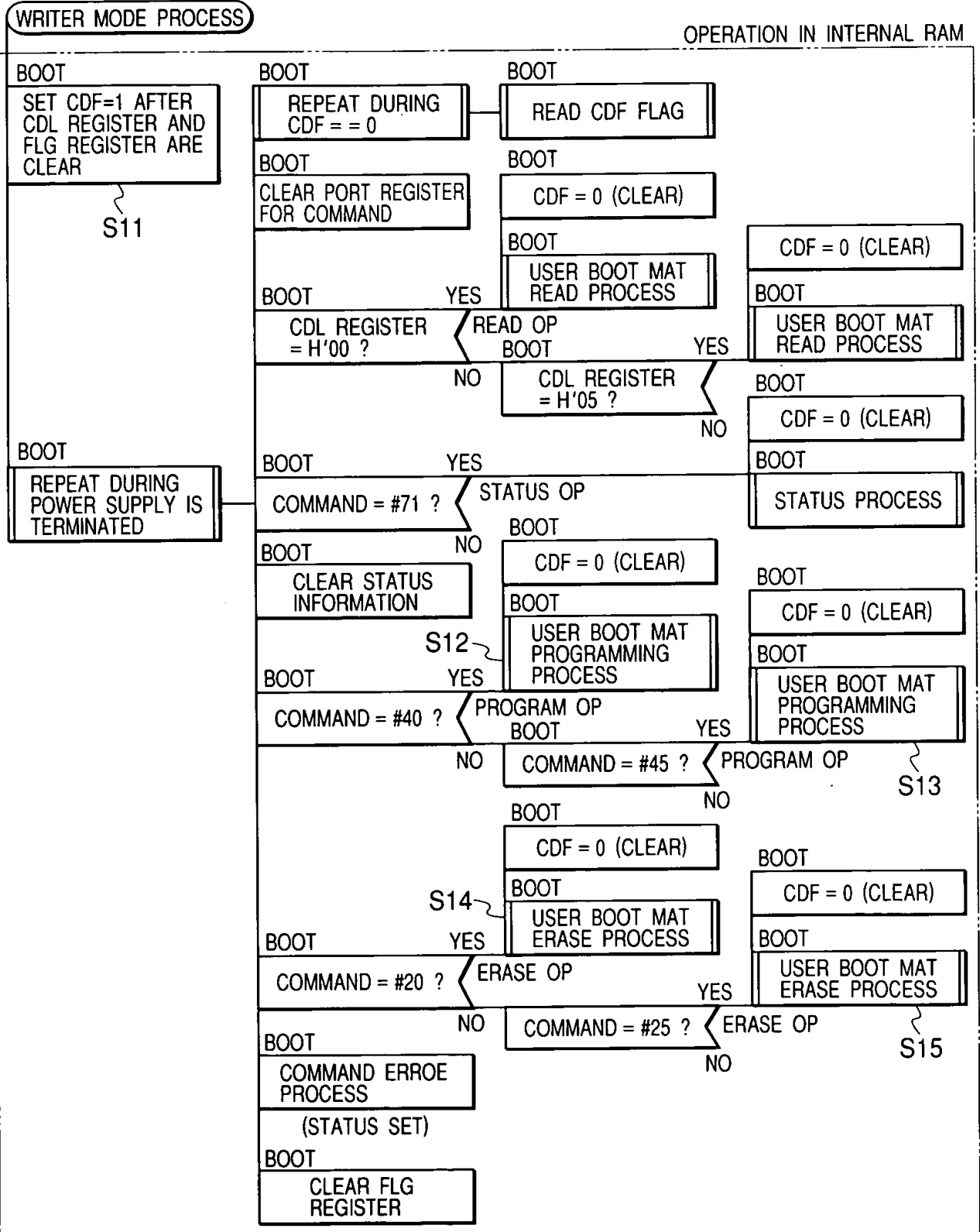


FIG. 10

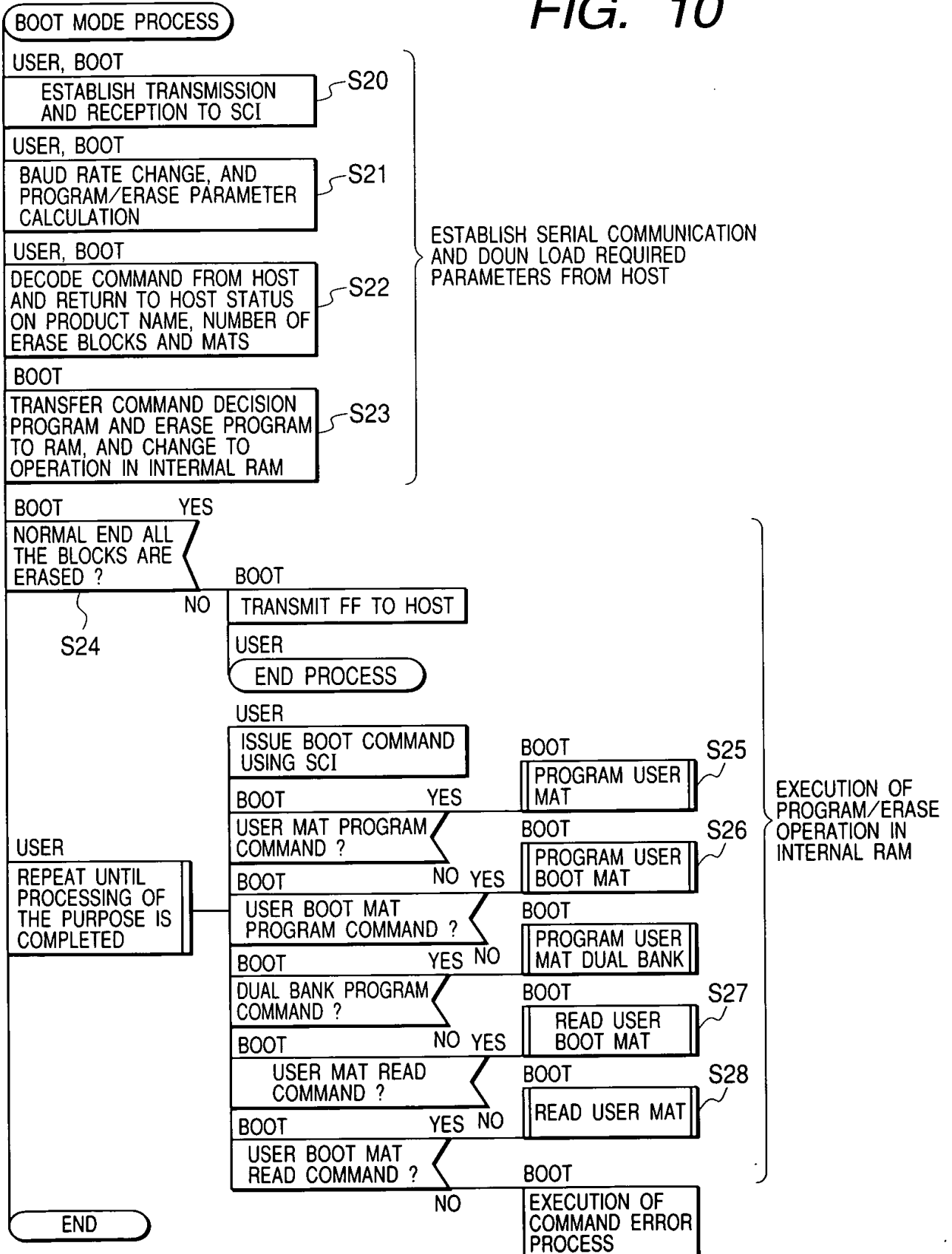


FIG. 11

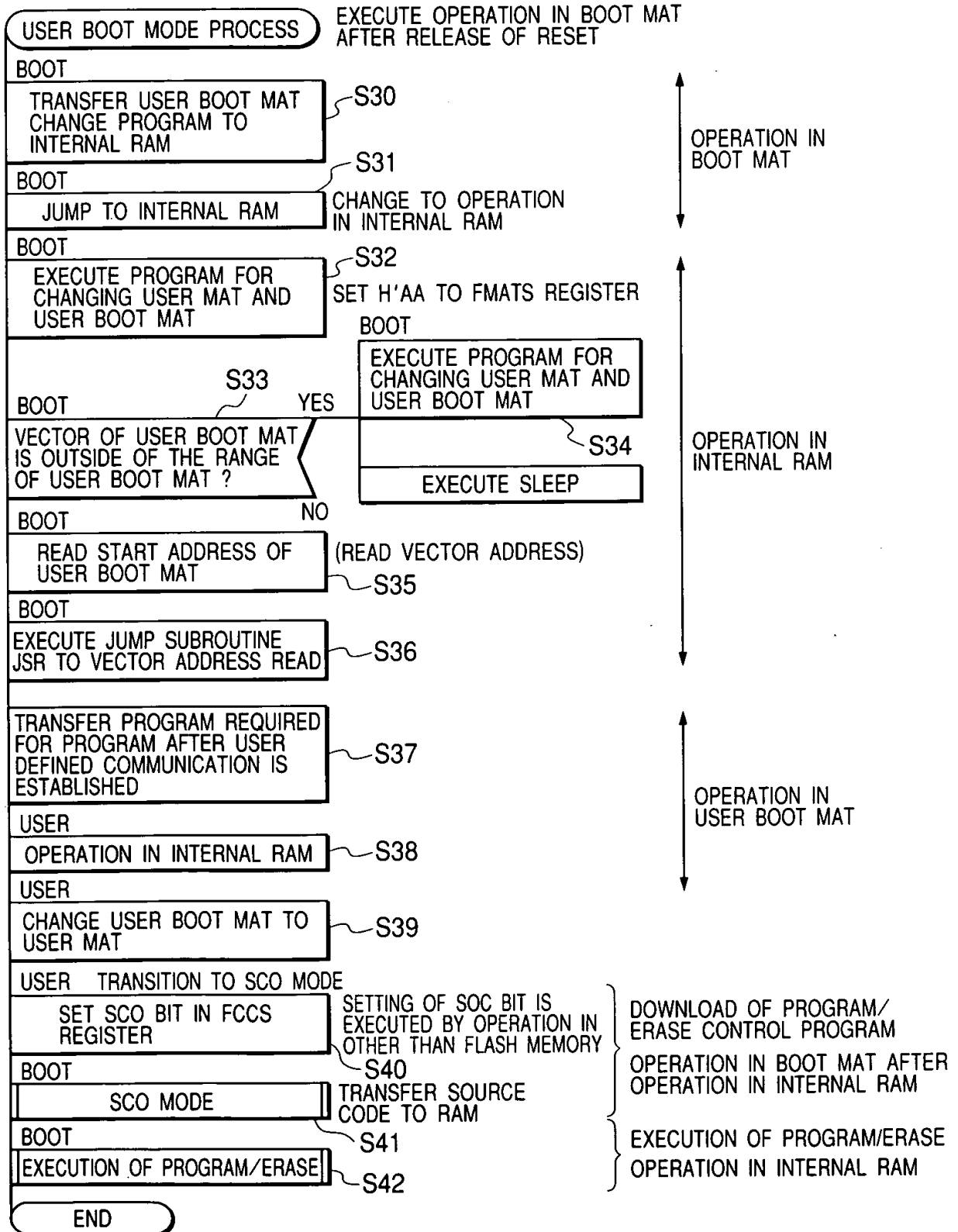


FIG. 12

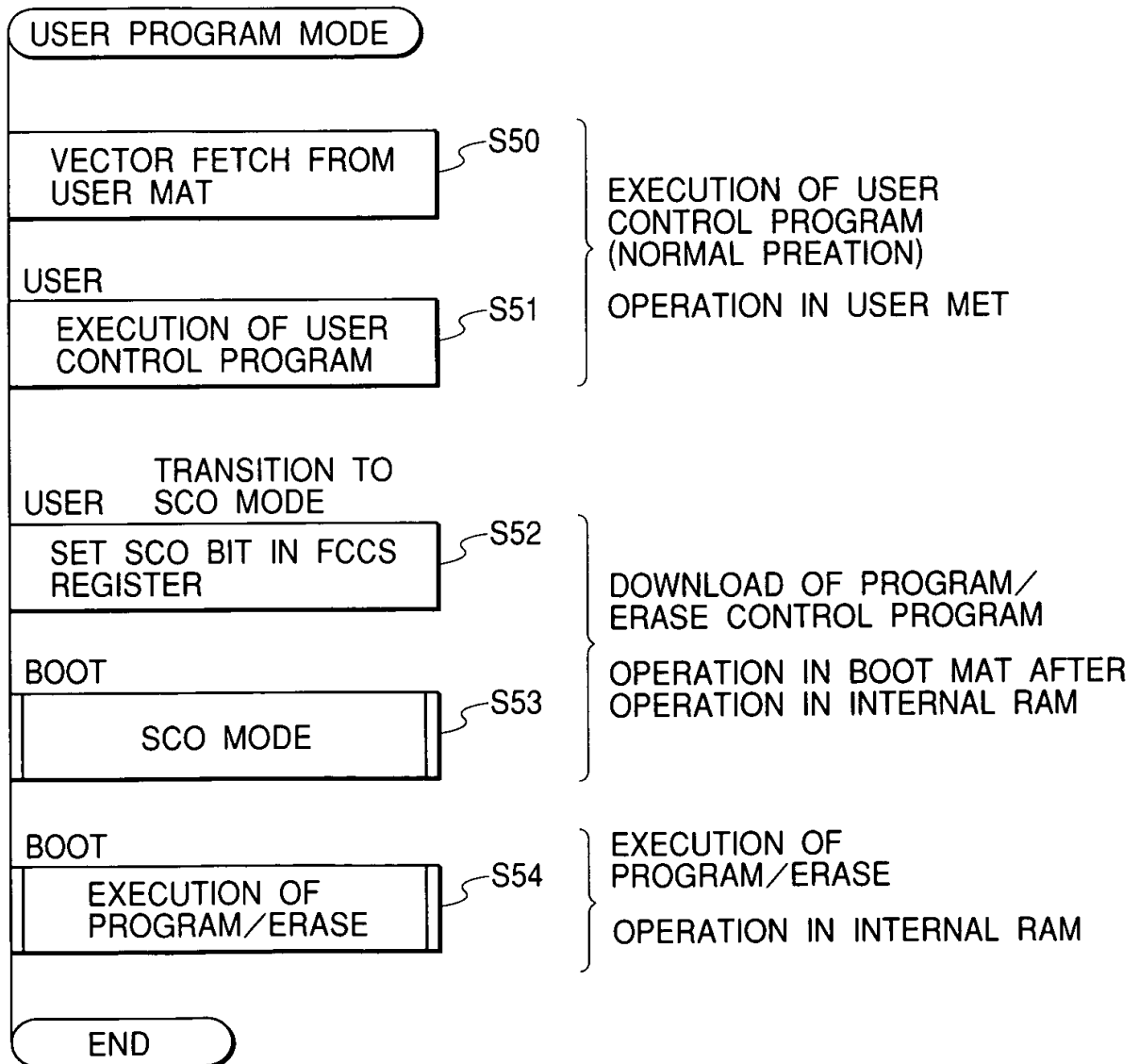


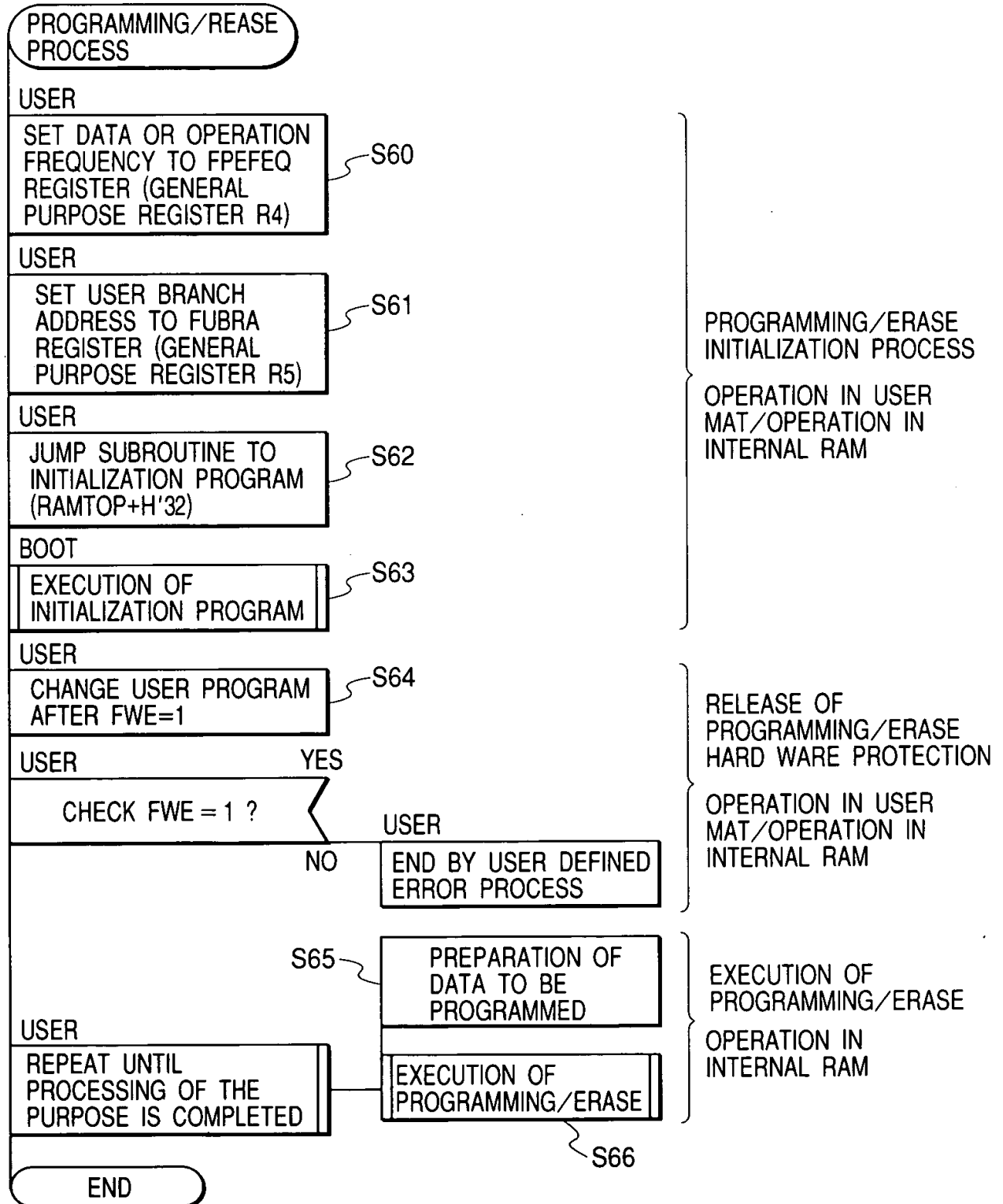
FIG. 13

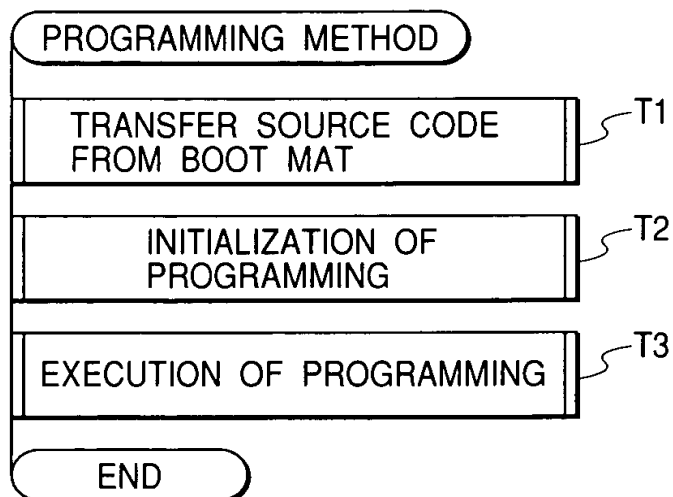
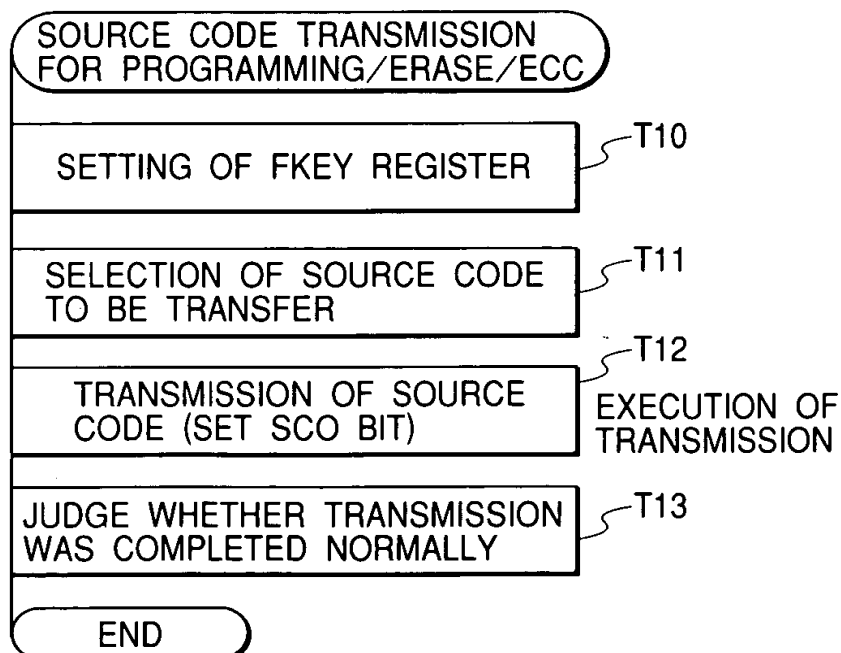
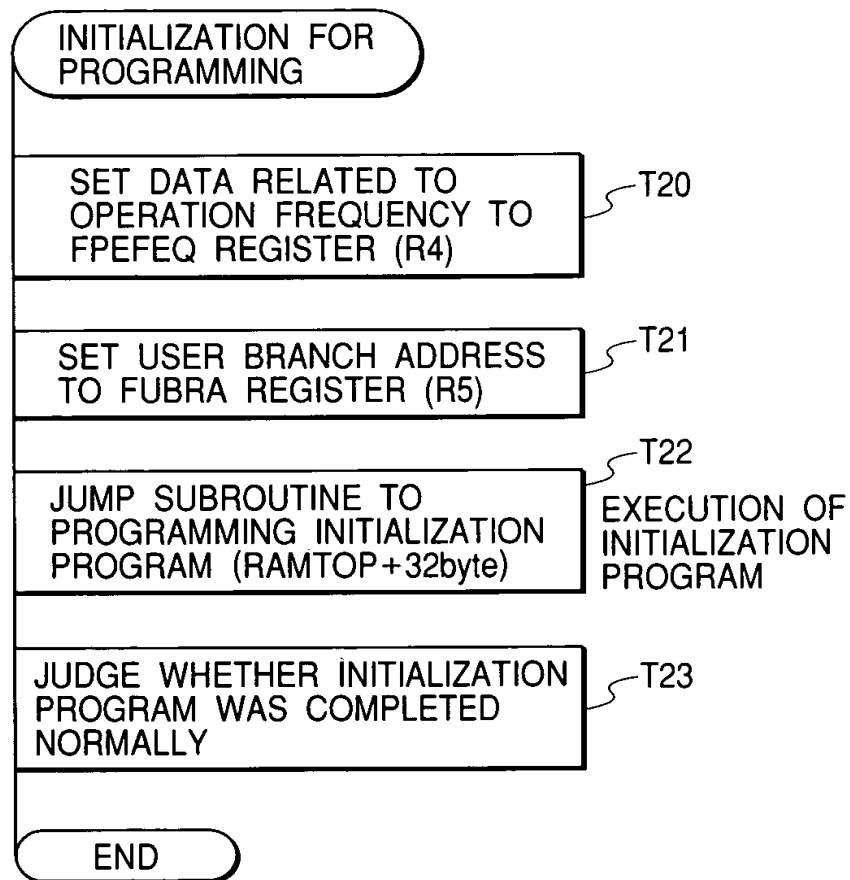
FIG. 14*FIG. 15*

FIG. 16

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graph TD
    Start([EXECUTION OF PROGRAMMING  
(PPVS, PPVD, ECPS)]) --> T30[T30]
    T30 --> S1[CHANGE BRANCH ADDRESS FOR  
PROCESSING NMI TO ADDRESS  
OF INTERNAL RAM]
    S1 --> T31[T31]
    T31 --> S2[INHIBIT INTERRUPT EXCEPT FOR  
NMI USING SR REGISTER]
    S2 --> T32[T32]
    T32 --> S3[SET SETTING AREA FOR WRITE  
ADDRESS TO R5]
    S3 --> T33[T33]
    T33 --> S4[SET SETTING AREA FOR  
ADDRESS OF WRITE DATA TO  
R4]
    S4 --> T34[T34]
    T34 --> S5[SET PROGRAM/ERASE CODE  
TO FKEY REGISTER]
    S5 --> T35[T35]
    T35 --> S6[JUMP SUBROUTINE TO  
PROGRAMMING PROGRAM  
(RAMTOP + 16byte)]
    S6 --> T36[T36]
    T36 --> S7[JUDGE WHETHER PROGRAMMING  
WAS COMPLETED NORMALLY]
    S7 --> End([END])

```

—T30
PLACE USER DEFINED
ERROR PROCESSING
ROUTINE TO INTERNAL
RAM

T31

T32

T33

T34

T35
EXECUTION OF
PROGRAMMING

T36

FIG. 18

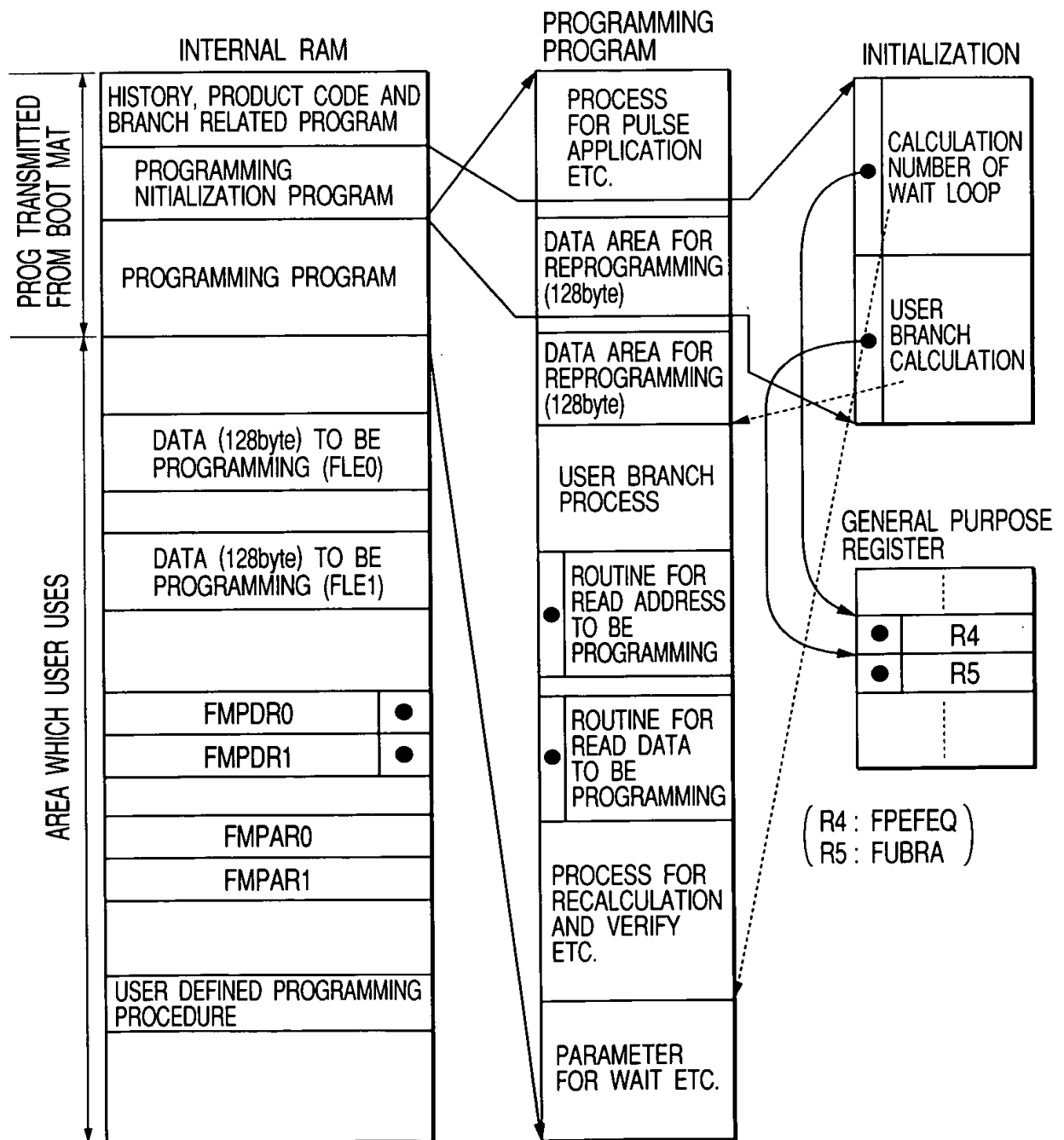


FIG. 19

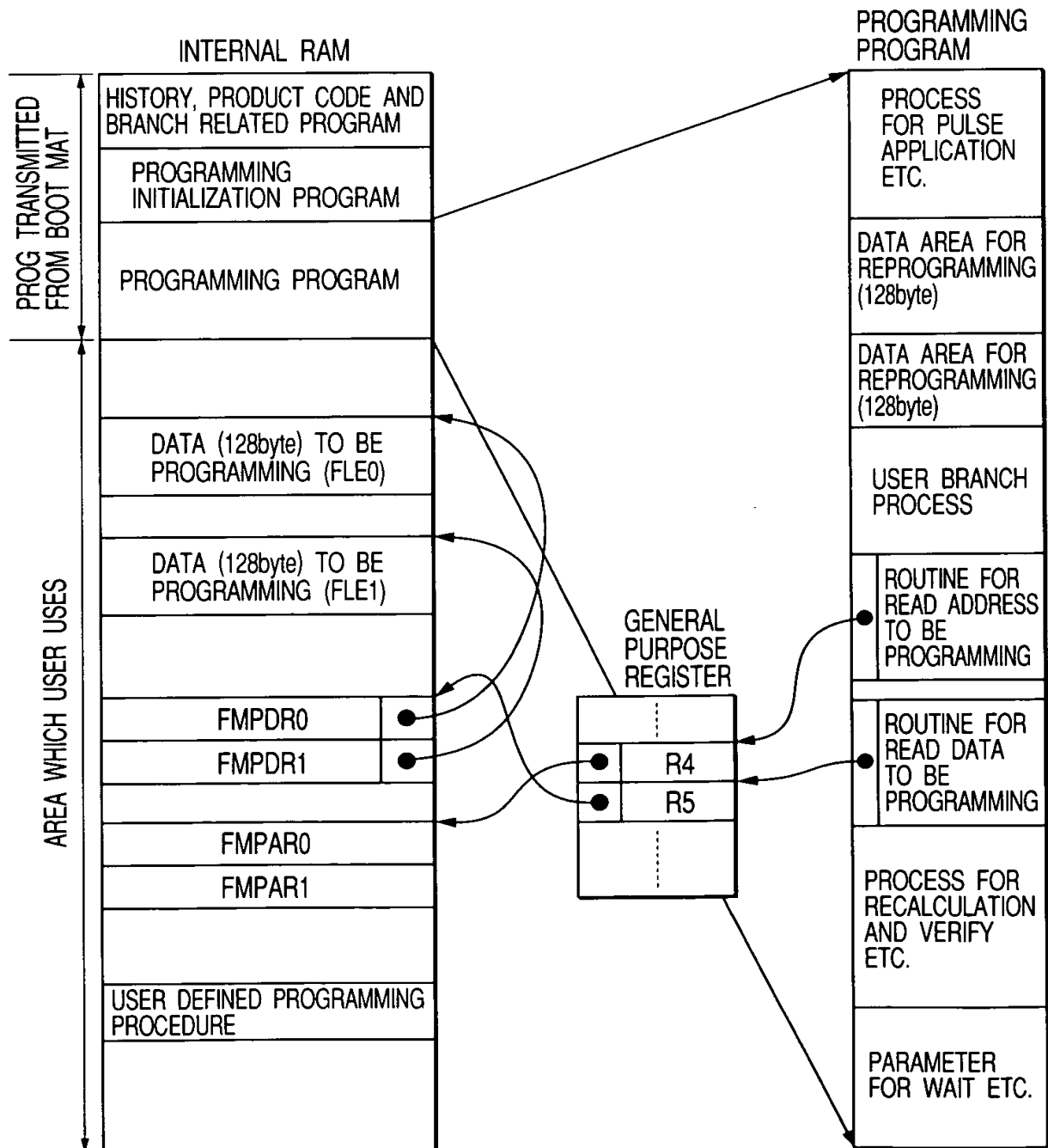


FIG. 20

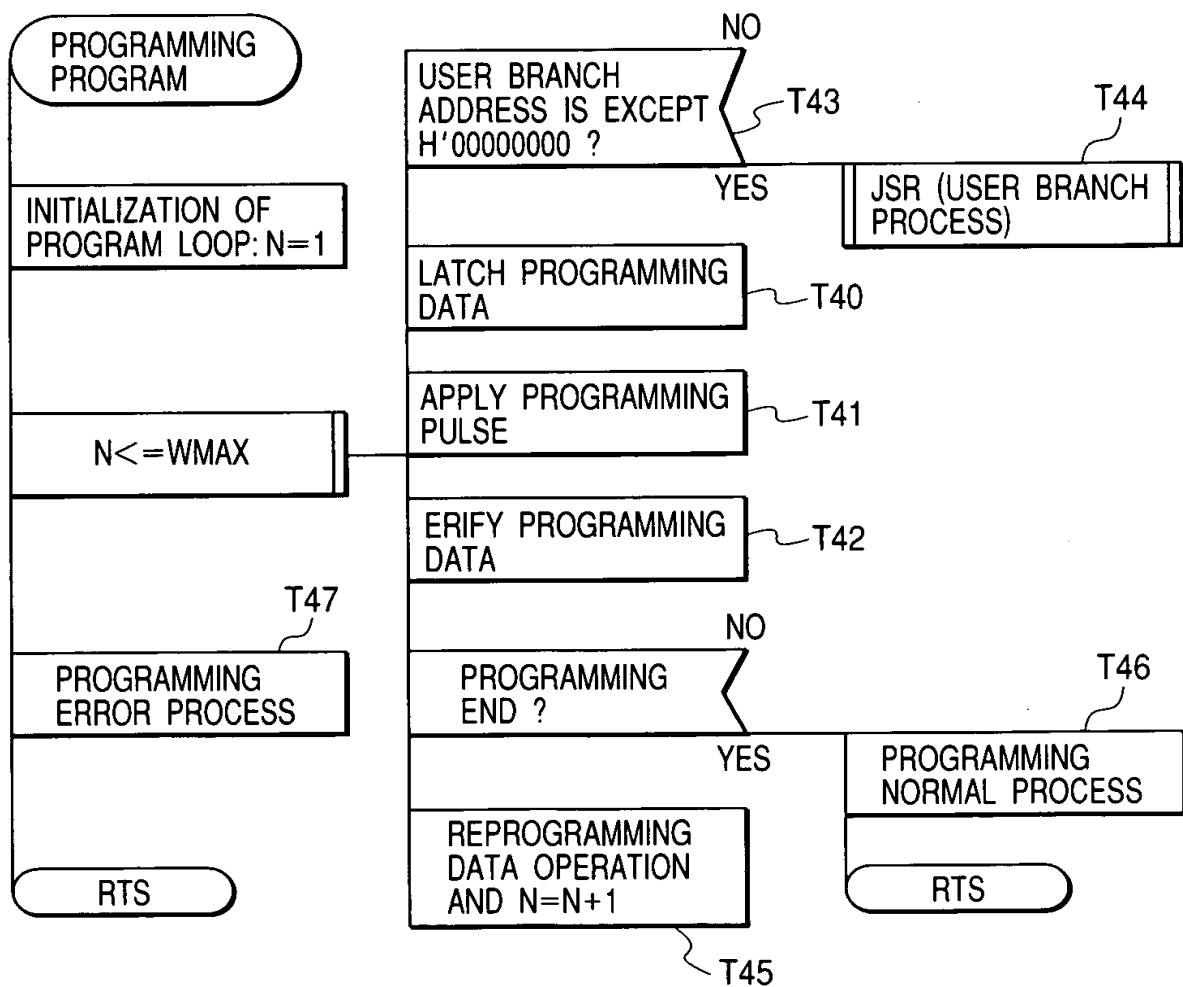


FIG. 21

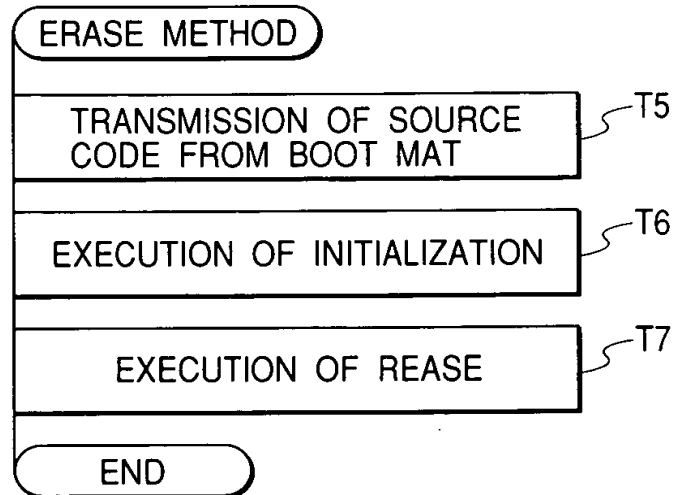
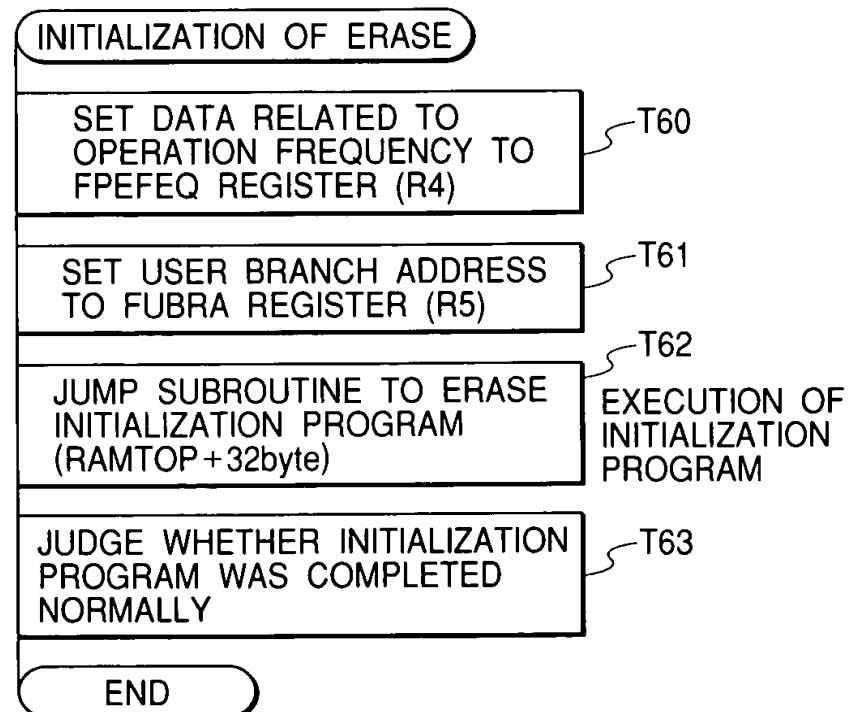
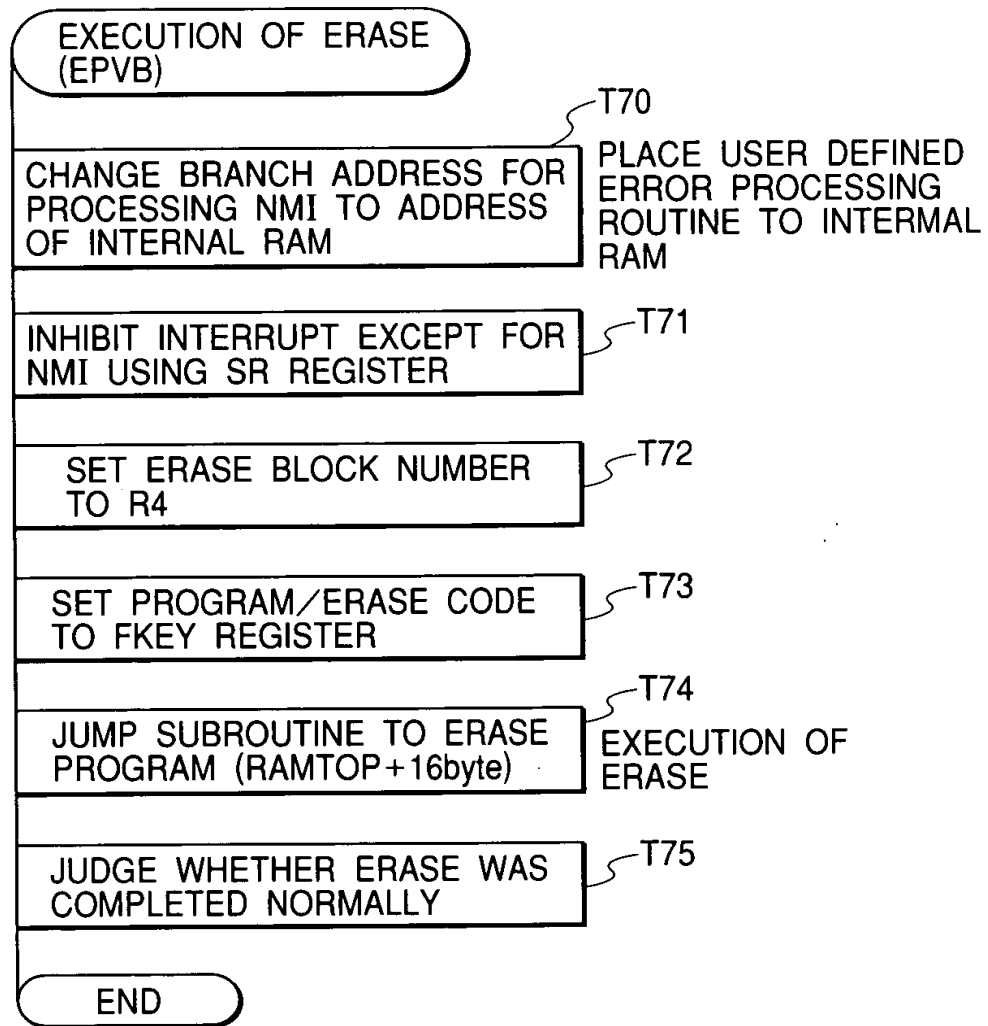


FIG. 22



202501180001

FIG. 23



20250310 19990902

FIG. 24

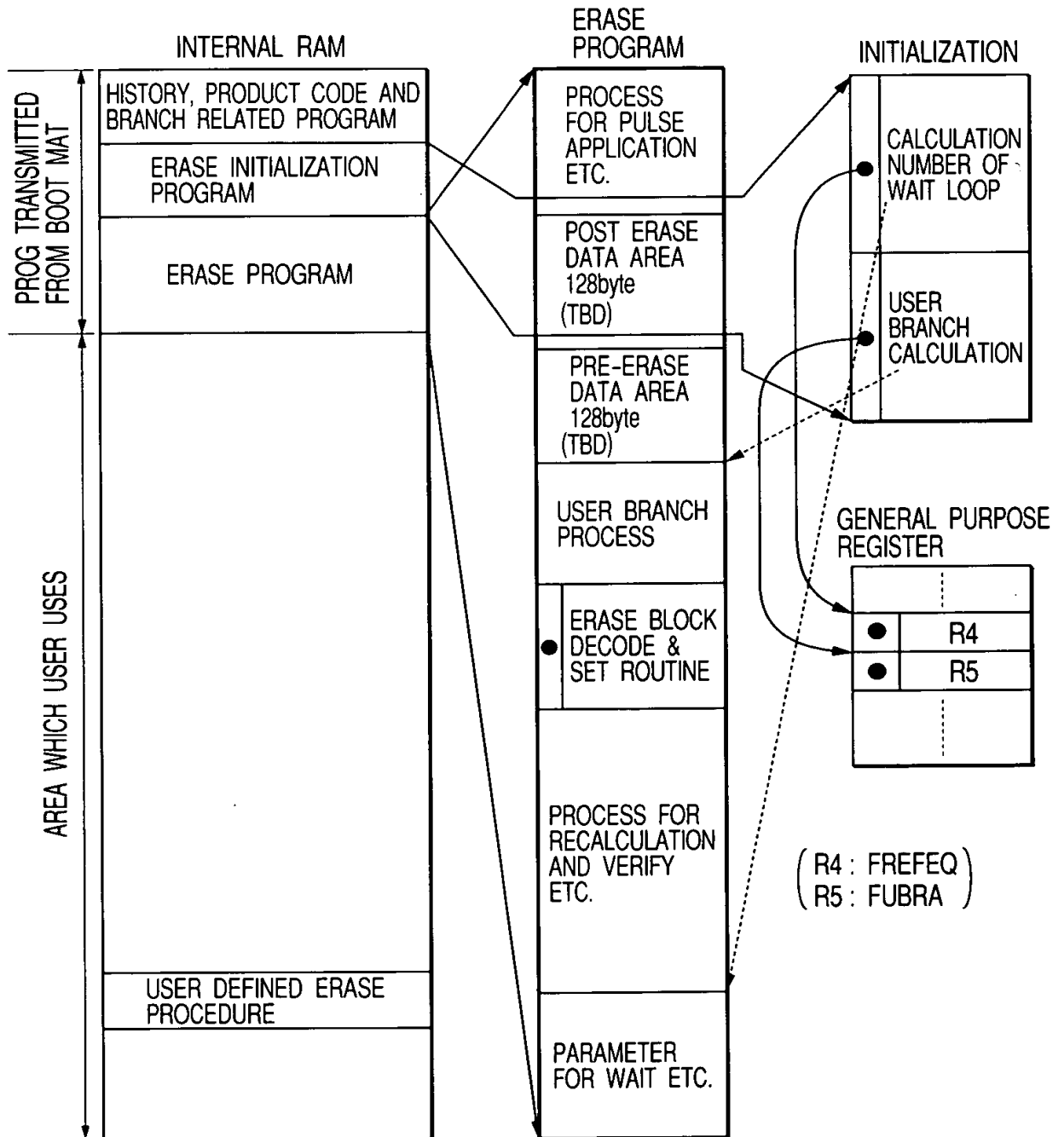


FIG. 25

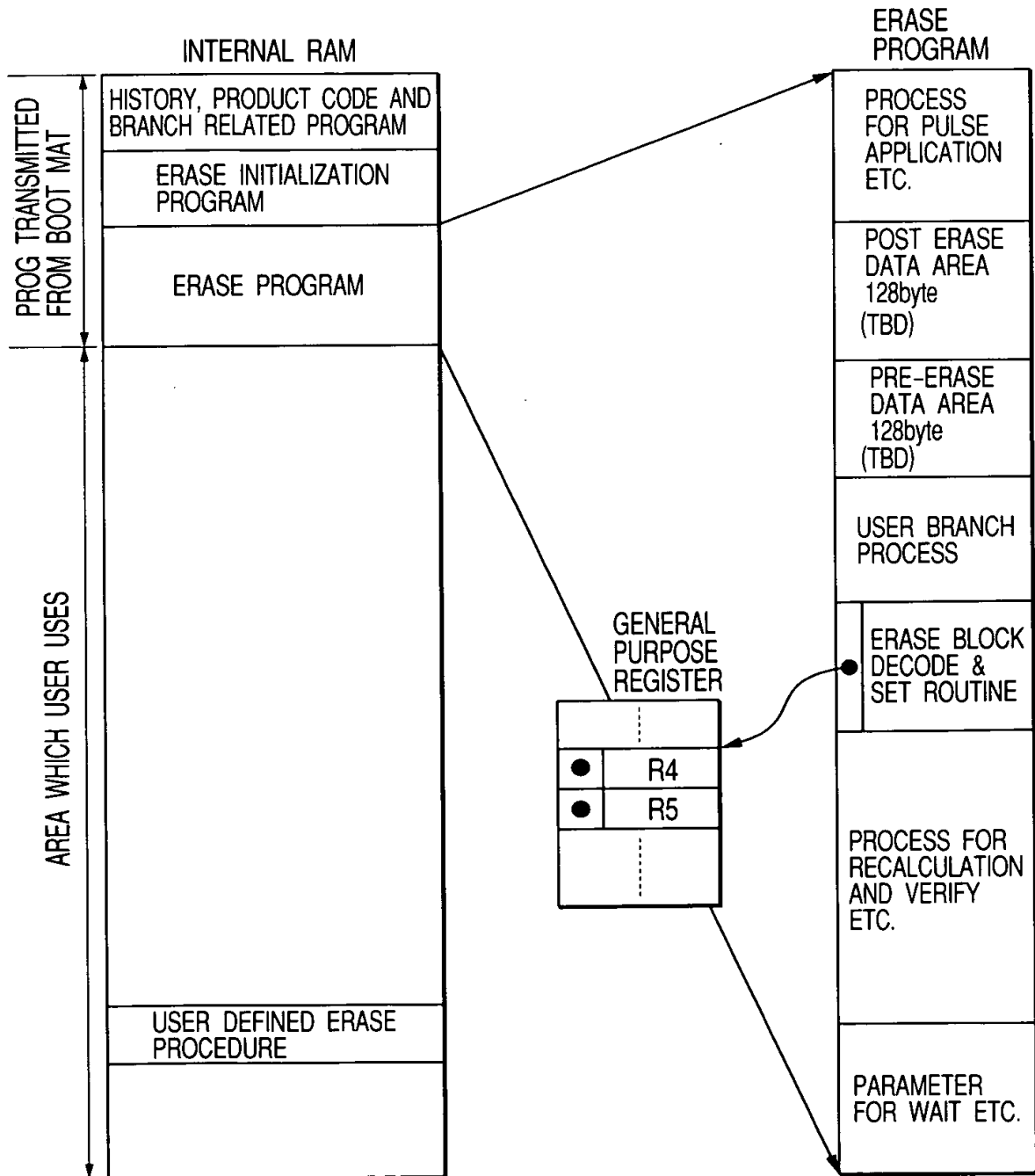


FIG. 26

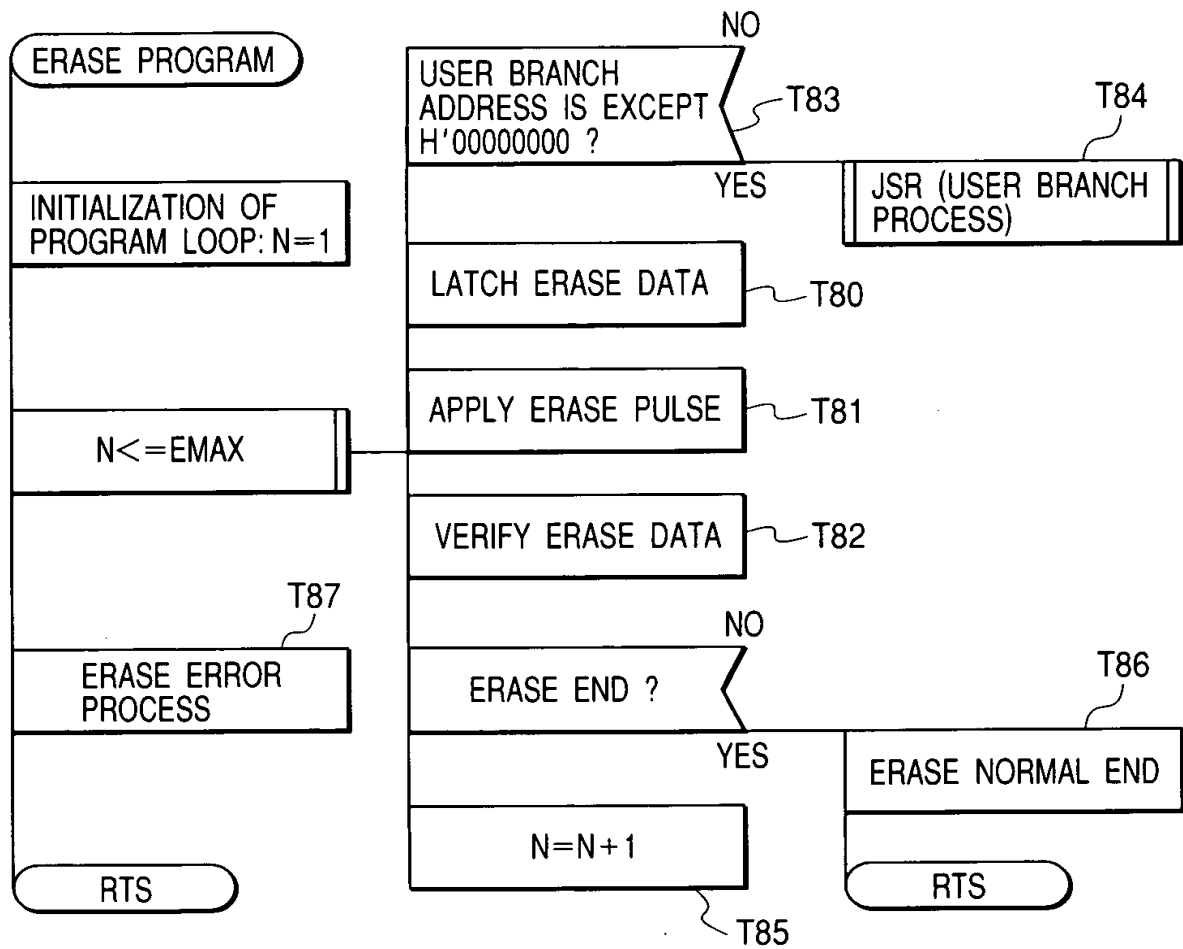


FIG. 27

